depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate, wherein amplifying the input signal comprises chopping the input signal utilizing a first NMOS depletion mode chopping switch responsive to a first chopping signal to produce a first chopped input signal; and

generating at least one opposite node of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal, and the level shifted first chopping signal in response to a clock signal.

22. (once amended) A method for amplifying a signal comprising:

generating an input signal;

amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier responsive to a level shifted first chopping signal to produce a chopper-stabilized output signal output signal;

amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal;

amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage to produce an amplified chopped output signal; and

generating, at opposite nodes of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal and the level shifted first chopping signal in response to a clock signal.